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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,886	04/12/2004	Masakatsu Tsuchiaki	251344US2RD	2493

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EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 01/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,886	TSUCHIAKI ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *1-5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/25/04; 12/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of group II (claims 6-19) in the reply filed on 10/7/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). A complete reply to the final rejection must include cancellation of nonelected claims 1-5 or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119 (a)-(d).

Information Disclosure Statement

The information disclosure statement filed on 8/25/04; 12/17/04 has been considered.

Oath/Declaration

Oath/Declaration filed on 8/25/04 has been considered.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9, 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "an electrode of a metal material containing copper formed in the insulating layer" is indefinite because it is unclear. It is suggested to change to "a plug of a metal material containing copper formed in the insulating layer".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8, 10-13, 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Besser et al. (U.S. Patent No. 2003/0235984) in view of Lu et al. (U.S. Patent No. 2004/0061184).

Referring to figures 1, 3, Besser et al. teaches a semiconductor device comprising a semiconductor element including:

a gate electrode (130) formed on a silicon semiconductor substrate (100),

source and drain regions (120) formed at both sides of the gate electrode (130) in the silicon semiconductor substrate (100), and

a NiSi layer formed on the source and drain regions (see paragraphs# 23, claims 1, 9),

where a junction depth of the source and drain regions being from 20 nm to 60 nm from a lower surface of the NiSi layer, Ni atoms existing in the source and drain regions, and a concentration of the Ni atoms at the junction depth being at $1.6 \times 10^{14} cm^{-3}$ or less (see paragraphs# 46). Noted that it would have been obvious that annealing at the same temperature and the same time period would provide the same result, see the present invention paragraph# 77-78 for details).

Regarding to claim 7, the concentration of the Ni atoms in the silicon semiconductor substrate at a portion 10nm in depth from the lower surface of the NiSi layer is at $5x10^{18} cm^{-3}$ or more, and $3x10^{21}$ cm^{-3} or less (see paragraphs 45, it is noted that the same process would provide the same result).

Regarding to claims 10, 15, wherein the gate electrode is completely formed of the Nisi layer (noted that the same process would provide the same result, see paragraph# 45-46).

Regarding to claims 11, 16, wherein a plurality of the semiconductor elements are formed on the silicon semiconductor substrate, each being isolated by an insulating layer filling up shallow trenches (110) formed in the silicon semiconductor substrate (100, see figure 3, paragraph# 23).

Regarding to claims 18, 19, further comprising an insulating layer (135, silicon oxide gate) having a dielectric constant of 3.9 or more between the gate electrode and the silicon semiconductor substrate (noted that the same material would have the same dielectric constant).

However, the reference does not teach the specific depth range and the concentration range, depositing the silicon nitride film to cover the NiSi layer, and the copper film to form the plug.

It would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made to optimize the concentration and the depth range, since it has been held that where the general conditions of a claim are disclosed in the prior art (i.e.- the concentration and the depth range), discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233 (CCPA 1955).

The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- wherein the depth range from 20-60nm, and the concentration range) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form the any depth range, and the concentration range in process of Besser et al. because determining the optimum range involves only routine skill in the art to reduce leakage current.

Lu et al teaches:

Regarding to claims 8, 13, further comprising a silicon nitride layer (190) formed to cover the NiSi layer (580/180/170, see figure 4) and to have an optical refractive index of 1.89 or less (noted that the same material would have the same optical refractive index).

Regarding to claims 12, 17, wherein n-type MOSFETS and p-type MOSFETS (CMOS, see paragraph# 20) constituting a logic circuit (see paragraph# 2, 20).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would from the silicon nitride on top of the NiSi layer and forming a n-type MOSFET and P-type MOSFETS constituting a logic circuit in process of Besser et al. as taught by Lu et al. because forming a silicon nitride film to protect the below active regions during the etching to form the opening, and forming the logic circuit to control output/input signal to the memory region.

Claims 9, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Besser et al. (U.S. Patent No. 2003/0235984) in view of Bohr (U.S. Patent No. 2004/0061184).

Besser et al. teaches forming a semiconductor device comprising a gate oxide, gate electrode, and a NiSi film. However the reference does not teach forming the copper containing plug. Nevertheless, forming the copper containing plug is known in the semiconductor as taught by Bohr.

Regarding to claims 9, 14, further comprising an insulating layer (21, silicon oxide) formed on the NiSi layer (19), and a plug of a metal material containing copper formed in the insulating layer for being electrically in contact with the NiSi layer.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would from the a plug by using copper containing material in process of Besser as taught by Bohr because forming the copper plug to contact output/input terminal to the circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, can be reached on (571) 272-1702. The fax phone number for this Group is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN